

IN THE CLAIMS

Please amend the claims as follows. Presented below is a complete listing of claims in the revised format showing markings as set forth by the U.S. Patent and Trademark Office on January 31, 2003:

1-12 (Canceled)

13. (Currently Amended) A method of making a symmetric transistor device comprising:

depositing a first conductive layer on a substrate, the first conductive layer forming an even number of transistor legs, laid out in an intersecting pattern, forming a bilaterally symmetric base;

doping the substrate to form source and drain regions and non-diffused areas around the intersections of the transistor legs; and

forming a plurality of transistors defined by a portion of a transistor leg forming a gate and the source and drain areas on either side of the leg forming a source and a drain.

14. (Original) The method of claim 13, further comprising:

depositing a silicon dioxide prior to depositing the first conductive layer.

15. (Canceled)

16. (Original) The method of claim 13, wherein the intersecting pattern forms a tic-tac-toe pattern.

17. (Original) The method of claim 13, wherein the first conductive layer comprises polysilicon.

18. (Original) The method of claim 13, further comprising:
conductive interconnections between the source and drain areas to form a circuit.

19. (Original) The method of claim 13, wherein a first half of the transistors are oriented along a first axis and a second half of the transistors (N/2) oriented along a second axis orthogonal to the first half of the transistors.

20. (Original) The method of claim 19, wherein the minimum drawn W/L is used for each transistor leg.

21. (New) A method of making a symmetric transistor device comprising:
depositing a first conductive layer on a substrate, the first conductive layer forming an even number of transistor legs, laid out in an intersecting pattern, forming a bilaterally symmetric base;
doping the substrate to form source and drain regions; and
forming a plurality of transistors defined by a portion of a transistor leg forming a gate and the source and drain areas on either side of the leg forming a source and a drain, so as to reduce skew effects due to mask alignment and gate orientation.

22. (New) The method of claim 21, wherein a first half of the transistors are oriented along a first axis and a second half of the transistors (N/2) oriented along a second axis orthogonal to the first half of the transistors.

23. (New) The method of claim 21, wherein variations in threshold voltage are reduced.